



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/631,933	07/31/2003	Alan F. Benner	POU920030015US1	9641

7590 04/27/2005

Philmore H. Colburn, II Esq.  
Canton Colburn LLP  
55 Griffin Road South  
Bloomfield, CT 06002

EXAMINER

KANG, JULIANA K

ART UNIT PAPER NUMBER

2874

DATE MAILED: 04/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/631,933

Applicant(s)

BENNER ET AL.

Examiner

Juliana K. Kang

Art Unit

2874

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. ____. |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>7/31/03</u> . | 6) <input type="checkbox"/> Other: ____.  |

## DETAILED ACTION

### ***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

2. **Claims 1-3 and 5-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hudgins et al (U.S. Patent 6,270,262 B1) and further in view of Giboney et al (U.S. Patent 6,318,909 B1).**

Regarding claims 1, 5, 7, 8, 15, 16, and 18, Hudgins et al disclose an optoelectronic assembly for a computer system, comprising: an electronic chip set (46); a substrate (30b) in communication with the electronic chip set; an electrical signaling

Art Unit: 2874

medium (101, flexible circuit board) having a first end in signal communication with the substrate; an optoelectronic transducer (60) in signal communication with a second end of the electrical signaling medium wherein an electrical signal from the electronic chip set is communicated to the optoelectronic transducer via the substrate and the electrical signaling medium (see column 4 lines 40-63), and wherein the electronic chip set and the optoelectronic transducer share a common thermal path for cooling (see column 4 lines 27-30 and 44-46). Hudgins et al teach coupling the optoelectronic assembly module to an optical fiber (62) however, Hudgins et al is silent about an optical coupling guide. Giboney et al teach using an optical coupling guide (a set of alignment pins) for aligning an optical fiber ribbon to an optoelectronic assembly for a precise alignment. Thus it would have been obvious to one having ordinary skill in the art at the time the invention was made to use an optical coupling guide in Hudgins et al as taught by Giboney et al for optimum coupling efficiency.

Regarding claim 2, Hudgins et al show heat spreader (50) in thermal contact with the both the electronic chip set and the optoelectronic transducer (see column 4 lines 27-30 and 44-46 and Fig. 3).

Regarding claims 3 and 14, Hudgins et al teach using the optoelectronic assembly in airborne applications (requires computer systems) thus it would have been obvious to one having ordinary skill in the art at the time the invention was made to use various chips to perform various functions in Hudgins et al to process more complex applications.

Art Unit: 2874

Regarding claims 13 and 17, Hudgins et al teach using a plurality of optoelectronic transducers. Having the transducers being offset from one another in either vertical direction or a horizontal direction would have been obvious to reduce a crosstalk between the transducers.

Regarding claim 6, Hudgins et al teach an integrated circuit (64) and a laser (90).

Regarding claim 9-12 and 19-20, as described above Hudgins et al and Giboney et al teach the claimed limitations except for the flexible printed circuit board in communication with either the second major surface or the edge surface of the substrate. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have the flexible printed circuit board in communication with the second major surface or the edge surface of the substrate to make the device more compact and it has been held that rearranging parts of an invention involves only routine skill in the art. Hudgins et al and Giboney et al do not teach having a recess. Using a recess is well known in the art to provide more accurate alignment between two components. Thus, using a recess in Hudgins et al and Giboney et al would have been obvious to one having ordinary skill in the art at the time the invention was made for optimum alignment between the substrate and the printed circuit board.

3. **Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hudgins et al (U.S. Patent 6,270,262 B1) and Giboney et al (U.S. Patent 6,318,909 B1) as applied to claim 1 and further in view of Nakao et al (U.S. Patent 6,306,511 B1).**

As described above Hudgins et al and Giboney et al teach the claimed invention including the substrate (printed circuit board) except the substrate made of an organic or a ceramic material. Nakao et al teach using a ceramic material for a circuit board to make an electronic chip device more compact and light-weighted. Thus it would have been obvious to one having ordinary skill in the art at the time the invention was made to use any known suitable material including a ceramic material in Hudgins et al and Giboney et al as taught by Nakao et al to make the device more compact.

### ***Conclusion***

4. The prior art documents submitted by applicant have been considered and made of record (note the attached copy of form PTO-1449).
5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Stricot et al (U.S. Patent 6,767,142 B2), Galloway (U.S. Patent 5,539,848), Thomas et al (U.S. Patent 5,625,734) and Brezina et al (U.S. Patent 6,659,656 B2) teach an optoelectronic assembly.
6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Juliana K. Kang whose telephone number is (571) 272-2348. The examiner can normally be reached on Mon. & Fri. 10:00-6:00 and Tue. & Thur. 10:00-3:00.

Art Unit: 2874

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rod Bovernick can be reached on (571) 272-2344. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
**JULIANA KANG**  
**PRIMARY EXAMINER** 4/25/05